

# IR2172

## LINEAR CURRENT SENSING IC

### Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low IQBS allows the boot strap power supply
- Independent fast overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

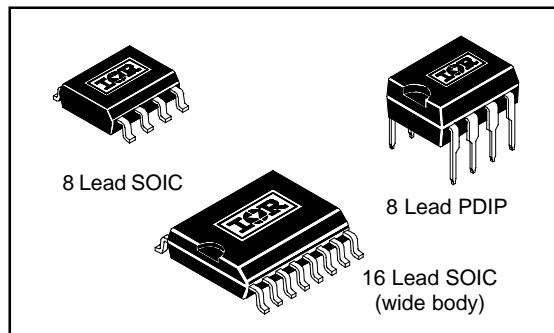
### Description

IR2172 is the monolithic current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM to eliminate need for the A/D input interface. The dedicated overcurrent trip (OC) signal facilitates IGBT short circuit protection. The OC output pulse can be programmed by the external resistor and capacitor. The open-drain outputs make easy for any interface from 3.3V to 15V.

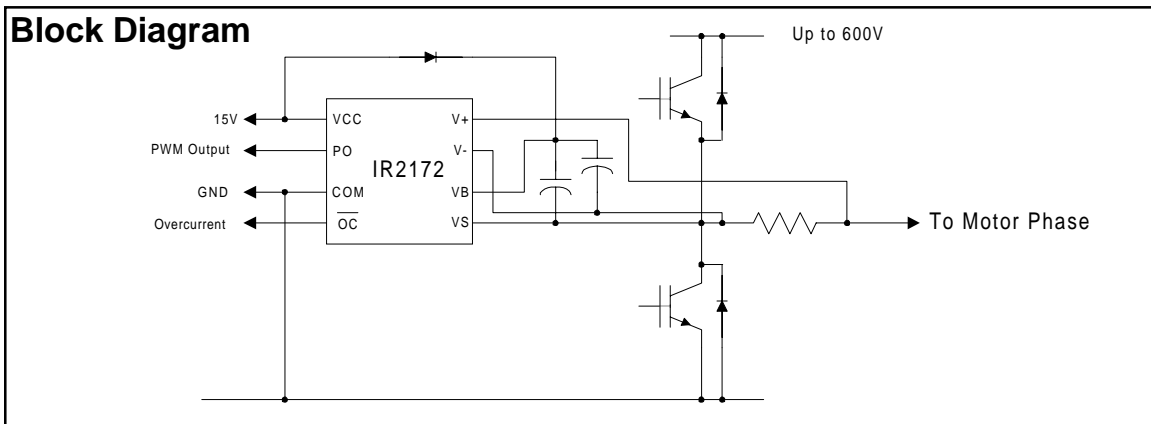
### Product Summary

$V_{\text{OFFSET}}$	600Vmax
$I_{\text{QBS}}$	1mA
$V_{\text{in}}$	+/-260mVmax
Gain temp.drift	20ppm/°C (typ.)
$f_0$	40kHz (typ.)
Overcurrent trip signal delay	1.5usec (typ)
Overcurrent trip level	+/-260mV (typ.)

### Packages



### Block Diagram



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>S</sub>	High side offset voltage	-0.3	600	V	
V <sub>BS</sub>	High side floating supply voltage	-0.3	25		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>IN</sub>	Maximum input voltage between V <sub>IN+</sub> and V <sub>IN-</sub>	-5	5		
V <sub>PO</sub>	Digital PWM output voltage	COM -0.3	V <sub>CC</sub> +0.3		
V <sub>OC</sub>	Overcurrent output voltage	COM -0.3	V <sub>CC</sub> +0.3		
V <sub>IN-</sub>	V <sub>IN-</sub> input voltage (note 1)	V <sub>S</sub> -5	V <sub>B+</sub> 0.3		
dV/dt	Allowable offset voltage slew rate	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
		16 lead SOIC	—	1.25	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
		16 lead SOIC	—	100	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: Capacitors are required between V<sub>B</sub> and V<sub>in-</sub>, and between V<sub>B</sub> and V<sub>S</sub> pins when bootstrap power is used. The external power supply, when used, is required between V<sub>S</sub> and V<sub>in-</sub>, and between V<sub>B</sub> and V<sub>S</sub> pins.

## Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High side floating supply voltage	V <sub>S</sub> +13.0	V <sub>S</sub> +20	V
V <sub>S</sub>	High side floating supply offset voltage	note 2	600	
V <sub>PO</sub>	Digital PWM output voltage	COM	V <sub>CC</sub>	
V <sub>OC</sub>	Overcurrent output voltage	COM	V <sub>CC</sub>	
V <sub>CC</sub>	Low side and logic fixed supply voltage	9.5	20	
V <sub>IN</sub>	Input voltage between V <sub>IN+</sub> and V <sub>IN-</sub>	-260	+260	mV
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 2: Logic operation for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## DC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$ , unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IN}$	Nominal input voltage range before saturation $ V_{IN+} - V_{IN-} $	-260	—	260	mV	
$V_{OC+}$	Overcurrent trip positive input voltage	—	260	—		
$V_{OC-}$	Overcurrent trip negative input voltage	—	-260	—		
$V_{OS}$	Input offset voltage	-10	0	10		$V_{IN} = 0V$ (Note 1)
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	$\mu V/^\circ C$	
G	Gain (duty cycle % per $V_{IN}$ )	157	162	167	%/V	max gain error=5% (Note 2)
$\Delta G/\Delta T_A$	Gain temperature drift	—	20	—	ppm/ $^\circ C$	
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	1	2	mA	$V_S = 0V$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	—	1		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta V_{LIN}/\Delta T_A$	Linearity temperature drift	—	.005	—	%/ $^\circ C$	
$I_{OPO}$	Digital PWM output sink current	20	—	—	mA	$V_O = 1V$
		2	—	—		$V_O = 0.1V$
$I_{OCC}$	OC output sink current	10	—	—		$V_O = 1V$
		1	—	—		$V_O = 0.1V$

Note 1:  $\pm 10mV$  offset represents  $\pm 1.5\%$  duty cycle fluctuation

Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

## AC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$ , unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
<b>Propagation delay characteristics</b>						
$f_o$	Carrier frequency output	—	40	—	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	500	—	ppm/ $^\circ C$	$V_{IN} = 0$ & $5V$
Dmin	Minimum duty	—	7	—	%	$V_{IN+} = -260mV, V_{IN-} = 0V$
Dmax	Maximum duty	—	93	—	%	$V_{IN+} = +260mV, V_{IN-} = 0V$
BW	$f_o$ bandwidth		15		kHz	$V_{IN+} = 100mV$ pk-pk sine wave, gain=-3dB
PHS	Phase shift at 1kHz		-10		$^\circ$	$V_{IN+} = 100mV$ pk-pk sine wave

### AC Electrical Characteristics cont.

$V_{CC} = V_{BS} = 15V$ , unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
<b>Propagation delay characteristics</b>						
tdoc	Propagation delay time of OC	1	1.5	—	μsec	
twoc	Low true pulse width of OC	—	1	—		

### Timing Waveforms

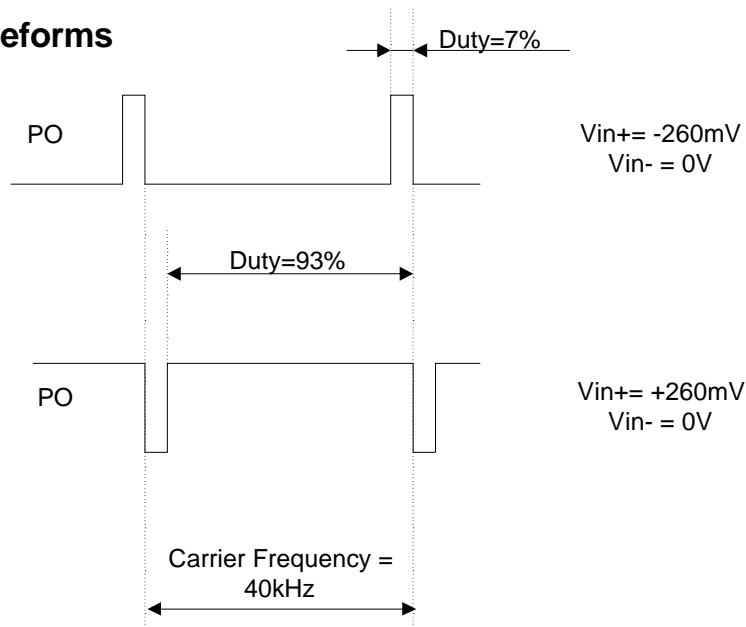


Figure 1 Output waveform

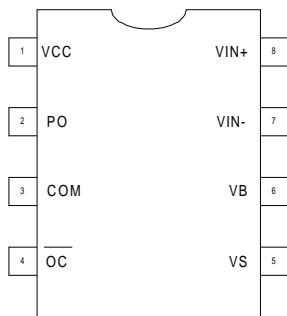
### Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at the same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM period gives consistent measurement of the current feedback over the temperature drift.

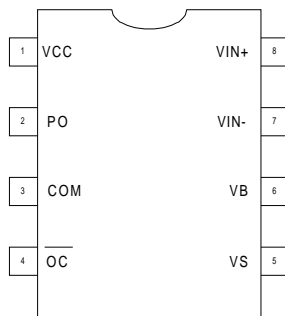
### Lead Definitions

Symbol	Description
VCC	Low side and logic supply voltage
COM	Low side logic ground
V <sub>IN+</sub>	Positive sense input
V <sub>IN-</sub>	Negative sense input
V <sub>B</sub>	High side supply
V <sub>S</sub>	High side return
PO	Digital PWM output
$\overline{OC}$	Overcurrent output (negative logic)
N.C.	No connection

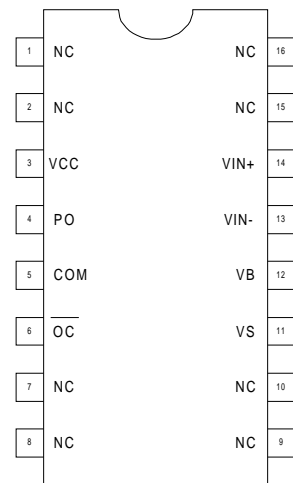
### Lead Assignment



8 lead SOIC  
IR2172S



8 lead PDIP  
IR2172



16 lead SOIC  
IR21726S

### Case Outline - 8 Lead SOIC

