



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating supply voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
I <sub>OMAX</sub>	Maximum allowable output current (HO, LO) due to external power transistor miller effect	-500	500	mA	
V <sub>VDC</sub>	VDC pin voltage	-0.3	V <sub>CC</sub> + 0.3	V	
V <sub>CT</sub>	CT pin voltage	-0.3	V <sub>CC</sub> + 0.3		
I <sub>CPH</sub>	CPH pin current	-5	5	mA	
I <sub>RPH</sub>	RPH pin current	-5	5		
V <sub>RPH</sub>	RPH pin voltage	-0.3	V <sub>CC</sub> + 0.3	V	
I <sub>RT</sub>	RT pin current	-5	5	mA	
V <sub>RT</sub>	RT pin voltage	-0.3	V <sub>CC</sub> + 0.3	V	
V <sub>CS</sub>	Current sense pin voltage	-0.3	5.5		
I <sub>CS</sub>	Current sense pin current	-5	5	mA	
I <sub>SD</sub>	Shutdown pin current	-5	5		
I <sub>CC</sub>	Supply current (note 1)	-20	20		
dV/dt	Allowable offset voltage slew rate	-50	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C P <sub>D</sub> = (T <sub>JMAX</sub> - T <sub>A</sub> ) / R <sub>thJA</sub>	(14 pin PDIP)	—	1.70	W
		(14 pin SOIC)	—	1.00	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(14 pin PDIP)	—	70	°C/W
		(14 pin SOIC)	—	120	
T <sub>J</sub>	Junction temperature	-55	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

Note 1: This IC contains a zener clamp structure between the chip V<sub>CC</sub> and COM which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V<sub>CLAMP</sub> specified in the Electrical Characteristics section.

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>BS</sub>	High side floating supply voltage	V <sub>CC</sub> - 0.7	V <sub>CLAMP</sub>	V
V <sub>BSMIN</sub>	Minimum required VBS voltage for proper HO functionality	5	V <sub>CC</sub>	
V <sub>S</sub>	Steady state high side floating supply offset voltage	-1	600	
V <sub>CC</sub>	Supply voltage	V <sub>CCUV+</sub>	V <sub>CLAMP</sub>	
I <sub>CC</sub>	Supply current	note 2	10	mA
C <sub>T</sub>	CT lead capacitance	220	—	pF
I <sub>SD</sub>	Shutdown lead current	-1	1	mA
I <sub>CS</sub>	Current sense lead current	-1	1	
T <sub>J</sub>	Junction temperature	-40	125	°C
I <sub>SDLK</sub>	SD pin leakage current (@V <sub>SD</sub> =6V)	—	125	μA
I <sub>CSLK</sub>	CS pin leakage current (@V <sub>CS</sub> =3V)	—	25	

Note 2: Enough current should be supplied into the VCC lead to keep the internal 15.6V zener clamp diode on this lead regulating its voltage, V<sub>CLAMP</sub>.

## Electrical Characteristics

V<sub>CC</sub> = V<sub>BS</sub> = V<sub>BIAS</sub> = 14V +/- 0.25V, V<sub>VDC</sub> = Open, R<sub>T</sub> = 39.0kΩ, R<sub>PH</sub> = 100.0kΩ, C<sub>T</sub> = 470 pF, V<sub>CPH</sub> = 0.0V, V<sub>CS</sub> = 0.0V, V<sub>SD</sub> = 0.0V, C<sub>LO</sub>, HO = 1000pF, T<sub>A</sub> = 25°C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
<b>Supply Characteristics</b>						
V <sub>CCUV+</sub>	V <sub>CC</sub> supply undervoltage positive going threshold	10.5	11.5	12.5	V	V <sub>CC</sub> rising from 0V
V <sub>CCUV-</sub>	V <sub>CC</sub> supply undervoltage negative going threshold	8.5	9.5	10.5		V <sub>CC</sub> falling from 14V
V <sub>UVHYS</sub>	V <sub>CC</sub> supply undervoltage lockout hysteresis	1.5	2.0	3.0		
I <sub>QCCUV</sub>	UVLO mode quiescent current	50	120	200	μA	V <sub>CC</sub> = 11V
I <sub>QCCFLT</sub>	Fault-mode quiescent current	—	200	470		SD = 5.1V, or CS > 1.3V
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> supply current	—	1.0	1.5	mA	CT connected to COM V <sub>CC</sub> = 14V, RT = 15kΩ
I <sub>QCC50K</sub>	V <sub>CC</sub> supply current, f = 50kHz	—	1.0	1.5		RT = 15kΩ C <sub>T</sub> = 470 pF
V <sub>CLAMP</sub>	V <sub>CC</sub> zener clamp voltage	14.5	15.6	16.5	V	I <sub>CC</sub> = 5mA
<b>Floating Supply Characteristics</b>						
I <sub>QBS0</sub>	Quiescent VBS supply current	-5	0	5	μA	V <sub>HO</sub> = V <sub>S</sub> (C <sub>T</sub> = 0V)
I <sub>QBS1</sub>	Quiescent VBS supply current	—	30	50		V <sub>HO</sub> = V <sub>B</sub> (C <sub>T</sub> = 14V)
I <sub>LK</sub>	Offset supply leakage current	—	—	50	μA	V <sub>B</sub> = V <sub>S</sub> = 600V

# IR2156(S) & (PbF)

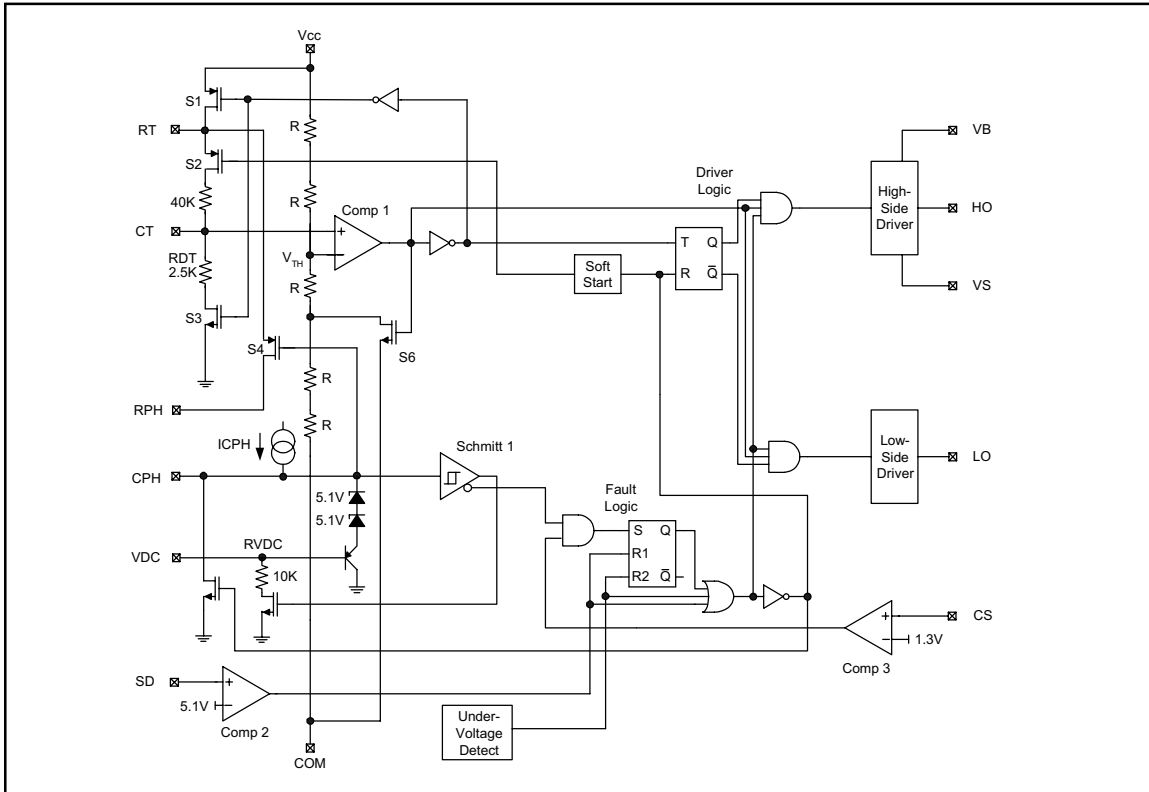
International  
IR Rectifier

## Electrical Characteristics

$V_{CC} = V_{BS} = V_{BIAS} = 14V \pm 0.25V$ ,  $V_{VDC} = \text{Open}$ ,  $R_T = 39.0k\Omega$ ,  $R_{PH} = 100.0k\Omega$ ,  $C_T = 470 \text{ pF}$ ,  $V_{CPH} = 0.0V$ ,  $V_{CS} = 0.0V$ ,  $V_{SD} = 0.0V$ ,  $C_{LO}, HO = 1000\text{pF}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
<b>Oscillator, Ballast Control, I/O Characteristics</b>						
$f_{osc}$	Oscillator frequency	28	30	32	kHz	$R_T=33.0k\Omega$ , $V_{VDC}=5V$ $V_{CPH} = \text{Open}$ (Guaranteed by design)
$f_{osc}$	Oscillator frequency	37.6	40	43.9	KHz	$R_T=40k$ , $R_{PH} = 100K$ $C_T = 470\text{pF}$
d	Oscillator duty cycle	—	50	—	%	
$V_{CT+}$	Upper $C_T$ ramp voltage threshold	—	8.3	—	V	$V_{CC} = 14V$
$V_{CT-}$	Lower $C_T$ ramp voltage threshold	—	4.8	—		
$V_{CTFLT}$	Fault-mode $C_T$ pin voltage	—	0	—	mV	$SD > 5.1V$ or $CS > 1.3V$ only CT CAP should beconnected to CT
$t_{DLO}$	LO output deadtime	—	2.0	—	usec	
$t_{DHO}$	HO output deadtime	—	2.0	—	usec	
RDT	Internal deadtime resistor	—	3	—	K $\Omega$	
<b>Preheat Characteristics</b>						
$I_{CPH}$	CPH pin charging current	3.6	4.3	5.2	$\mu\text{A}$	$V_{CPH}=10V, C_T=10V$ , $V_{DC}=5V$
$V_{CPHFLT}$	Fault-mode CPH pin voltage	—	0	—	mV	$SD > 5.1V$ or $CS > 1.3V$
<b>RPH Characteristics</b>						
$I_{RPHLK}$	Open circuit RPH pin leakage current	—	0.1	—	$\mu\text{A}$	$C_T = 10V$
$V_{RPHFLT}$	Fault-mode RPH pin voltage	—	0	—	mV	$SD > 5.1V$ or $CS > 1.3V$
<b>RT Characteristics</b>						
$I_{RTLK}$	Open circuit RT pin leakage current	—	0.1	—	$\mu\text{A}$	$C_T = 10V$
$V_{RTFLT}$	Fault-mode RT pin voltage	—	0	—	mV	$SD > 5.1V$ or $CS > 1.3V$
<b>Protection Characteristics</b>						
$V_{SDTH+}$	Rising shutdown pin threshold voltage	—	5.1	—	V	
$V_{SDHYS}$	Shutdown pin threshold hysteresis	—	450	—	mV	
$V_{CSTH}$	Over-current sense threshold voltage	1.1	1.25	1.44	V	
$t_{CS}$	Over-current sense propagation delay	—	160	—	nsec	Delay from CS to LO
$V_{CSPW}$	Over-current sense minimum pulse width	—	135	—	nsec	$V_{CS}$ pulse amplitude = $V_{CSTH}+100\text{mV}$
$R_{VDC}$	DC bus sensing resistor	7.5	10	14	k $\Omega$	$V_{CPH}>12V$ , $V_{CT}=0V$ $V_{DC}=7V$
$V_{CPH-VDC}$	CPH to VDC offset voltage	10.3	10.9	11.4	V	$V_{CPH}=\text{open}, V_{VDC}=0V$
<b>Gate Driver Output Characteristics</b>						
$V_{OL}$	Low-level output voltage	—	0	105	mV	$I_o = 0$
$V_{OH}$	High-level output voltage	—	0	100		$V_{BIAS} - V_o, I_o = 0$
$t_r$	Turn-on rise time	—	110	150	ns	$C_{LO} = C_{HO} = 1\text{nF}$
$t_f$	Turn-off fall time	—	55	100		

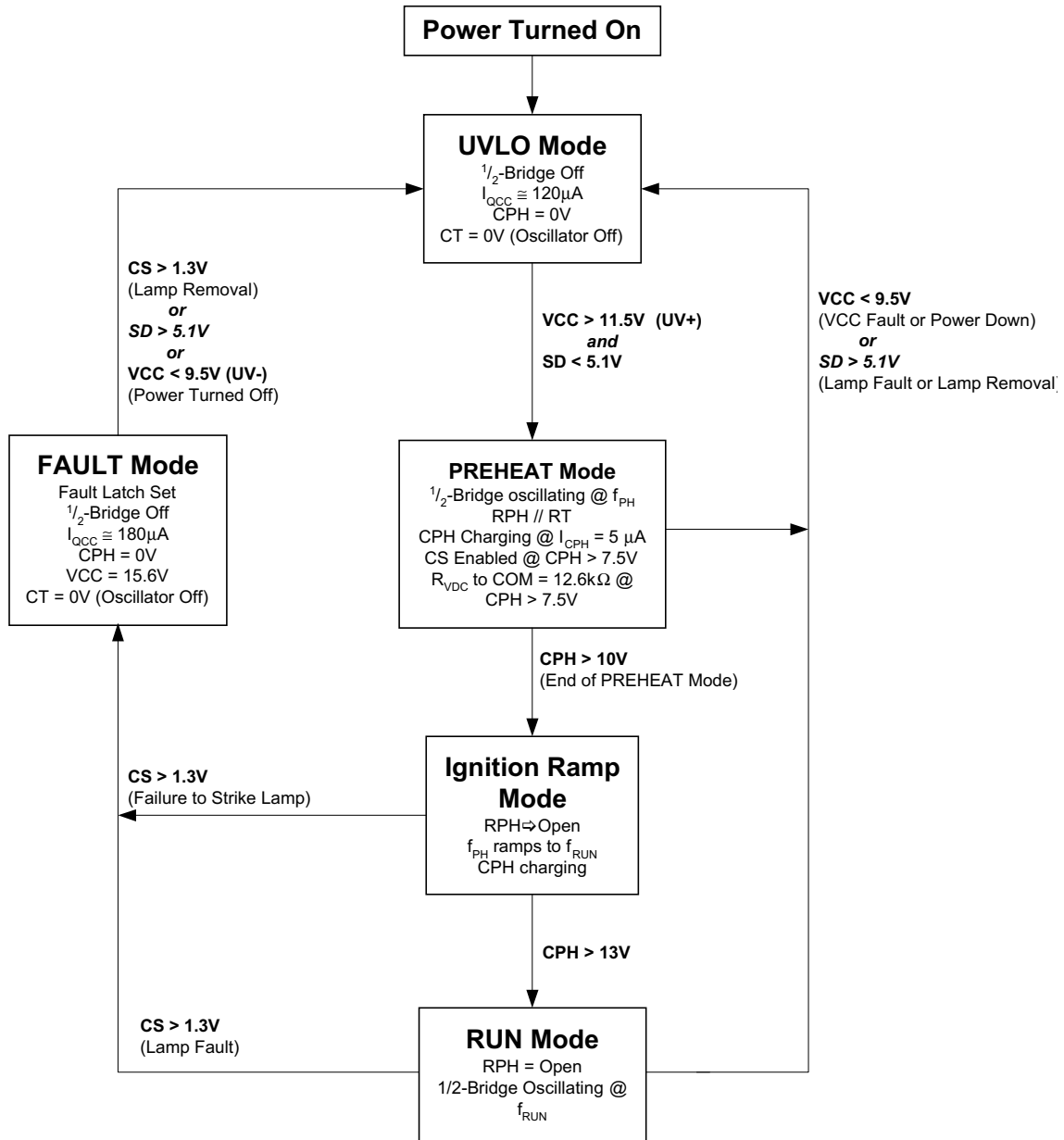
## Block Diagram



## Lead Assignments & Definitions

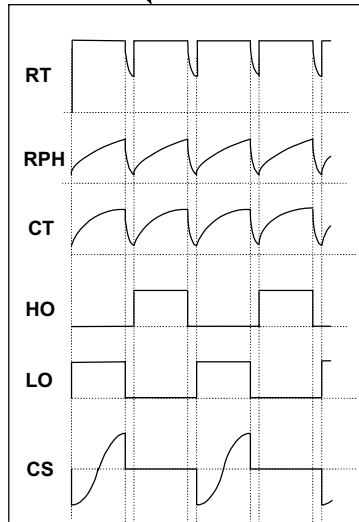
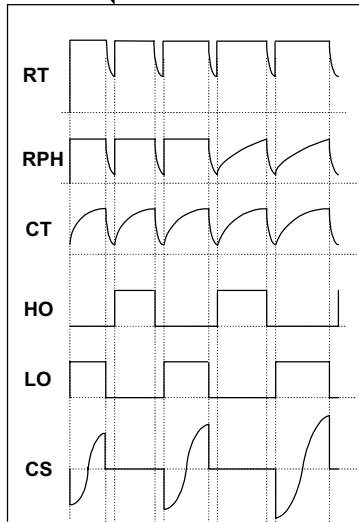
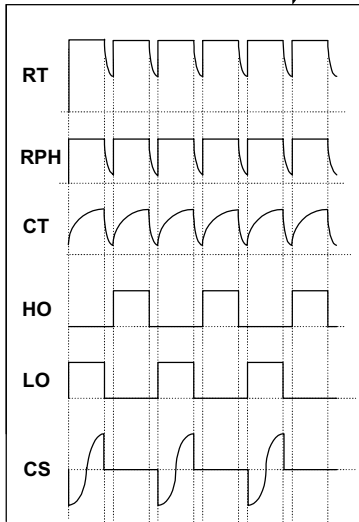
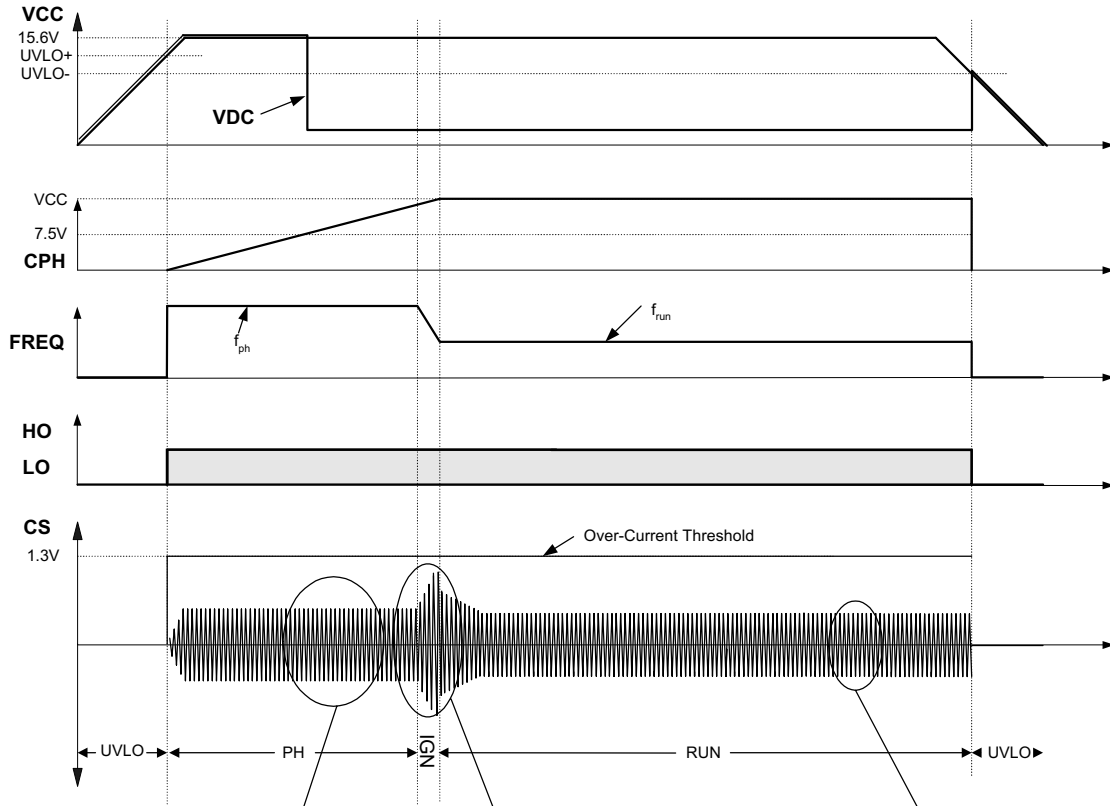
Pin Assignments		Pin #	Symbol	Description
NC	1	14	VB	No connect
VCC	2	13	HO	Logic & low-side gate driver supply
VDC	3	12	VS	IC start-up and DC bus sensing Input
RT	4	11	LO	Minimum frequency timing resistor
RPH	5	10	CS	Preheat frequency timing resistor
CT	6	9	SD	Oscillator timing capacitor
CPH	7	8	COM	Preheat timing capacitor
				IC power & signal ground
				Shutdown input
				Current sensing input
				Low-side gate driver output
				High-side floating return
				High-side gate driver output
				High-side gate driver floating supply

## State Diagram



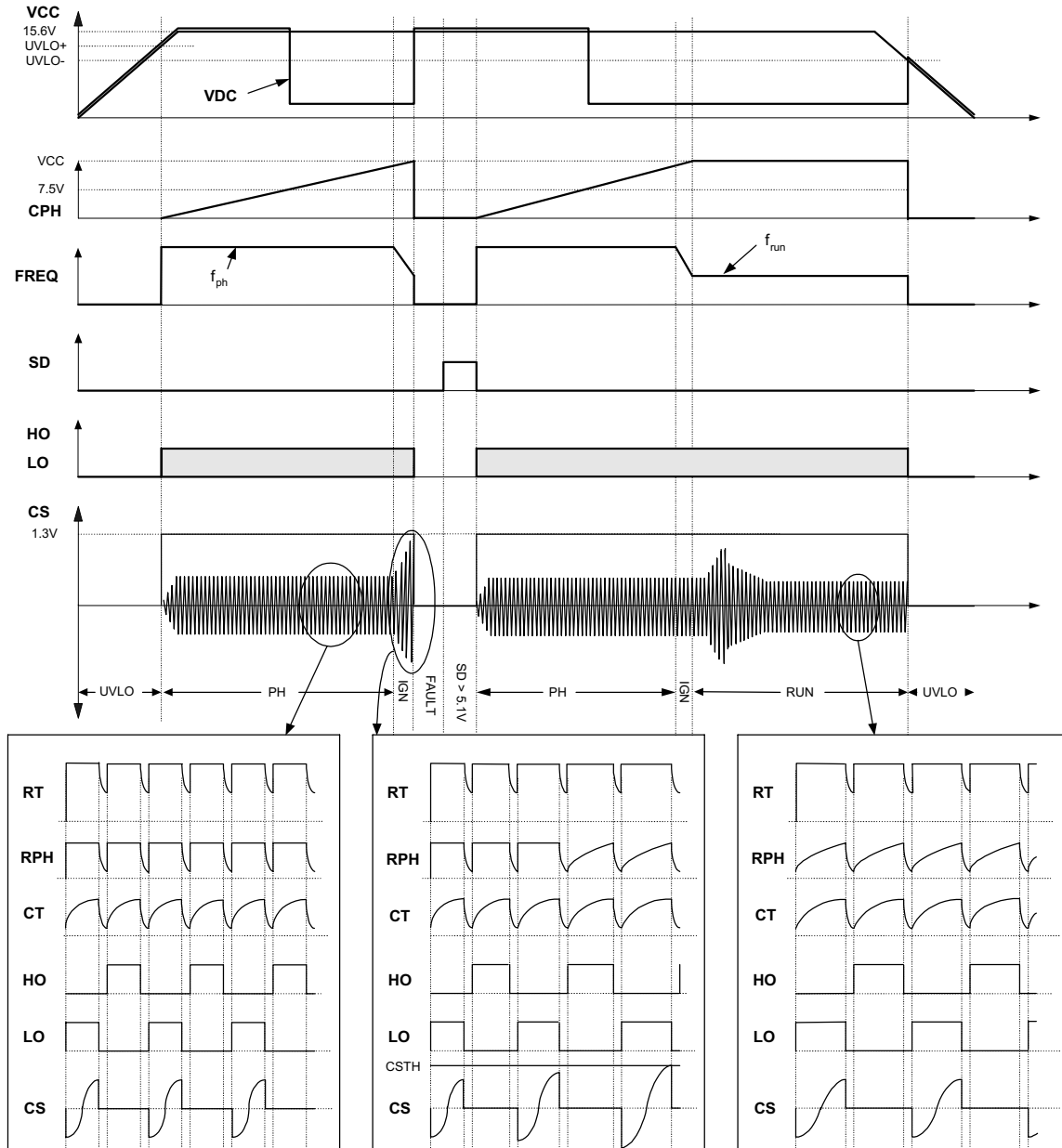
Timing Diagrams

Normal operation

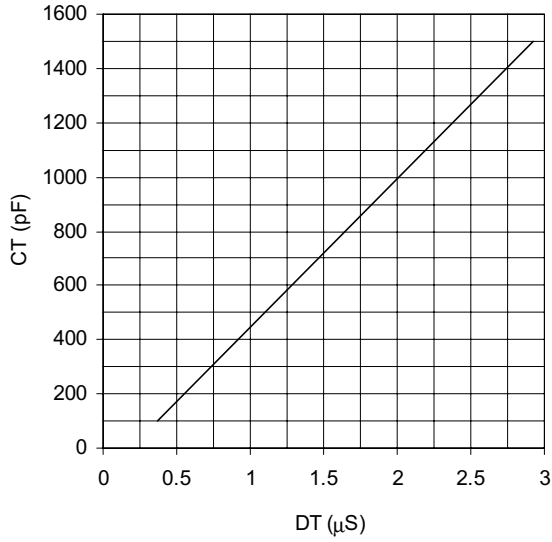


## Timing Diagrams

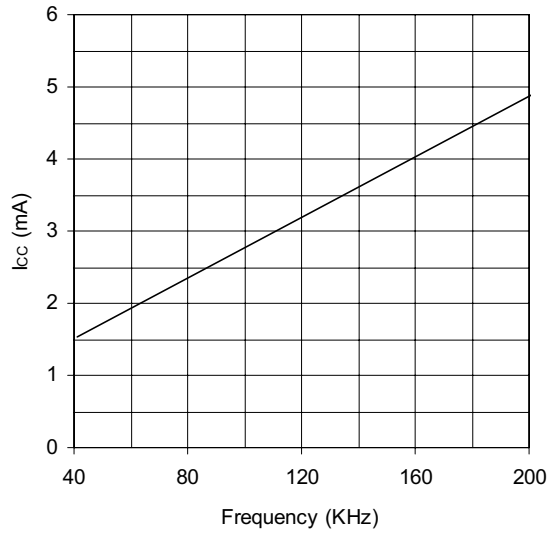
Fault condition



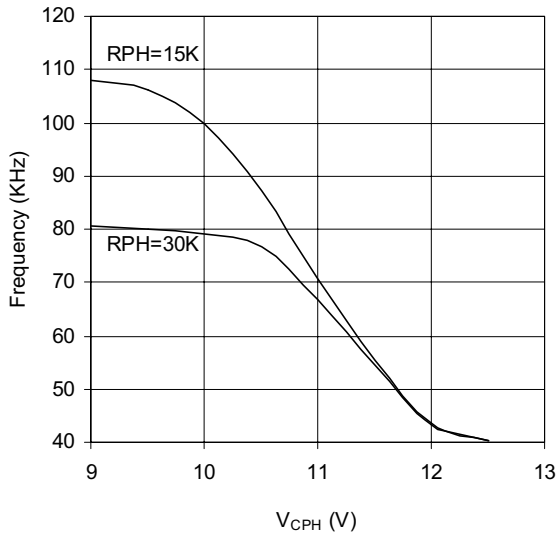




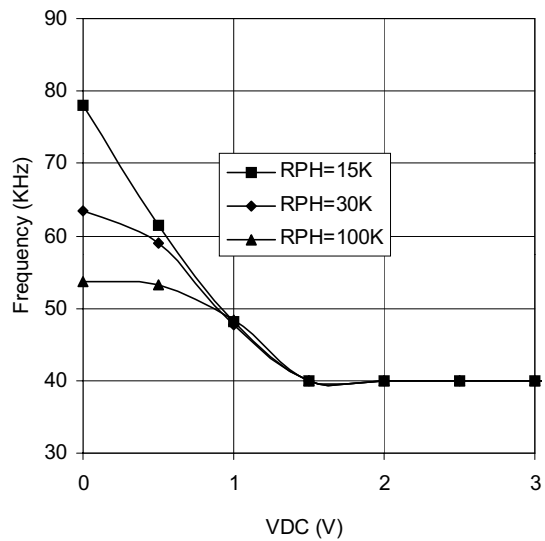
Graph 1. CT vs Dead Time (IR2156)



Graph 2. ICC vs Frequency (IR2156)

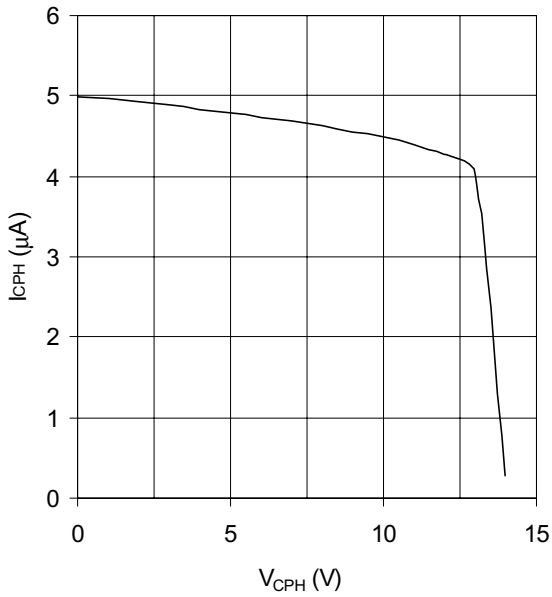


Graph 3. Frequency vs VCPH (IR2156)

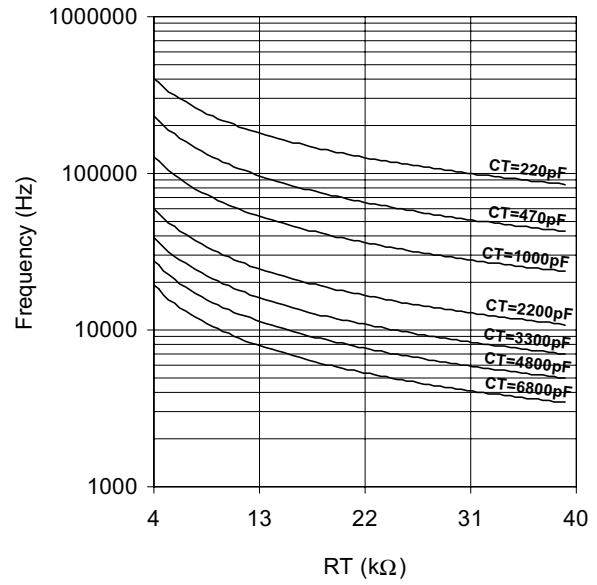


Graph 4. Frequency vs VDC (IR2156)

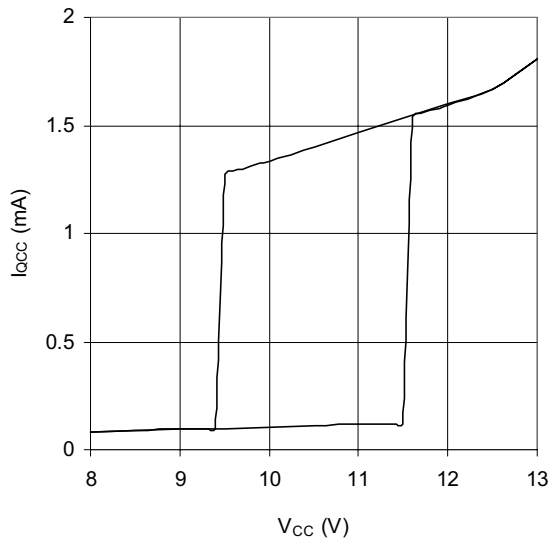
# IR2156(S) & (PbF)



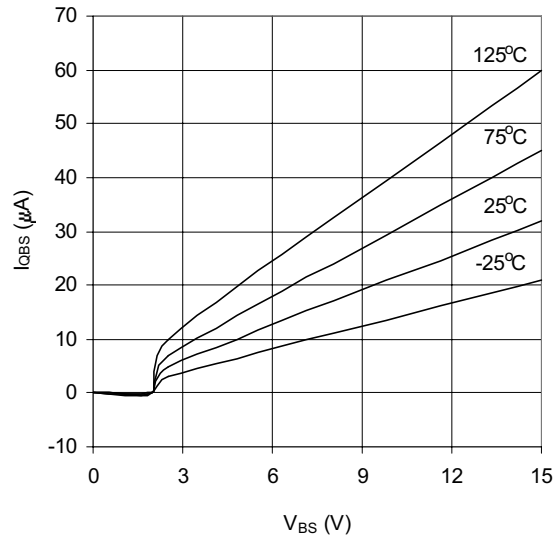
Graph 5.  $I_{CPH}$  vs  $V_{CPH}$  (IR2156)



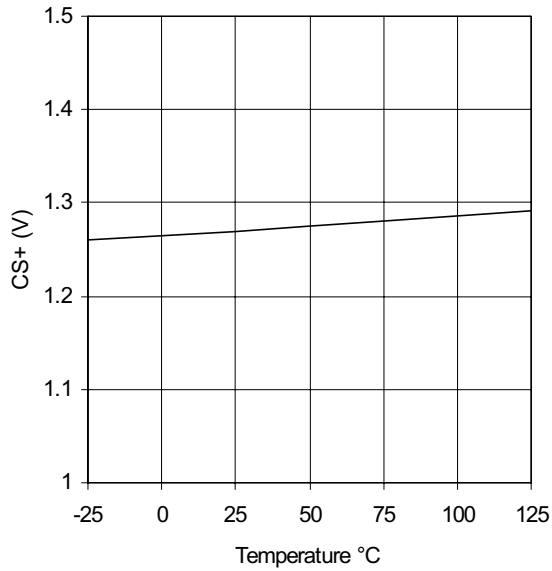
Graph 6. Frequency vs  $RT$  (IR2156)



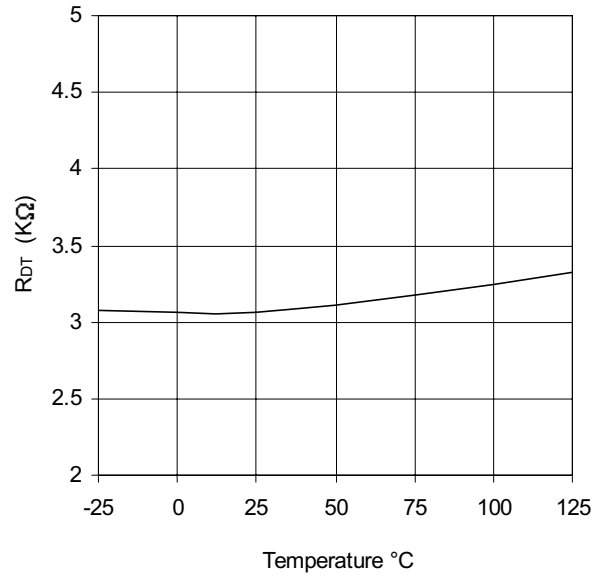
Graph 7.  $I_{QCC}$  vs  $V_{CC}$  (IR2156)  
UVLO Hysteresis



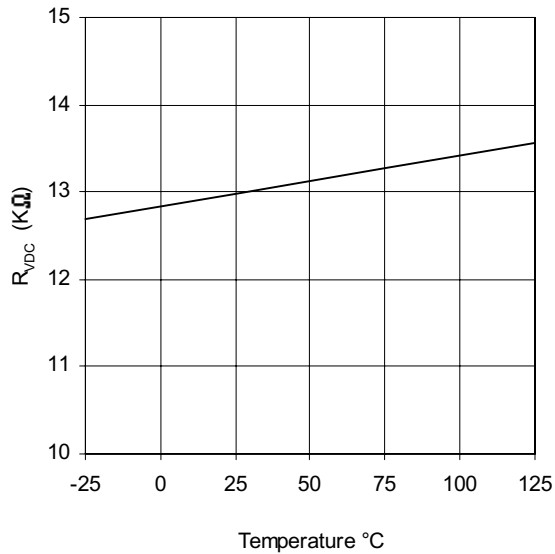
Graph 8.  $I_{QBS}$  vs  $V_{BS}$  vs Temp (IR2156)



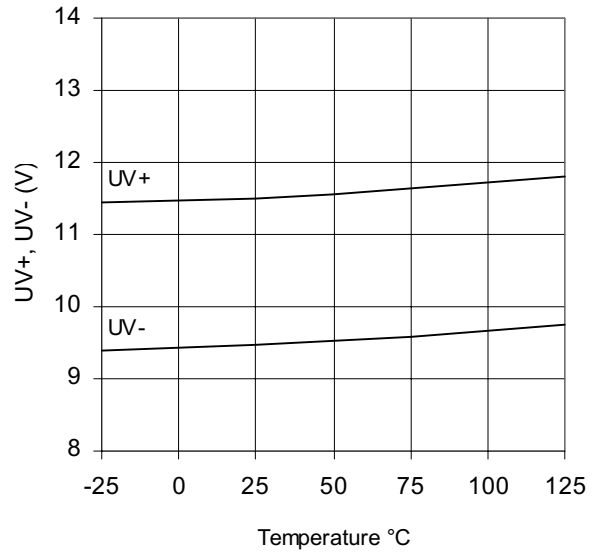
Graph 9.  $V_{CSTH+}$  vs Temperature (IR2156)



Graph 10.  $R_{DT}$  vs Temperature (IR2156)

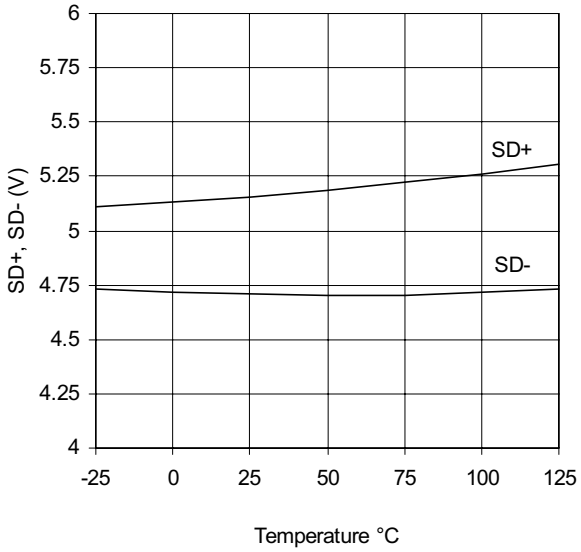


Graph 11.  $R_{VDC+}$  vs Temperature (IR2156)

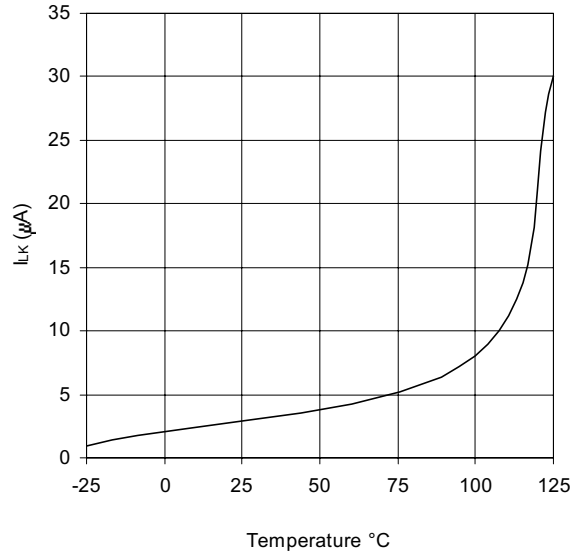


Graph 12.  $UV+$ ,  $UV-$  vs Temperature (IR2156)

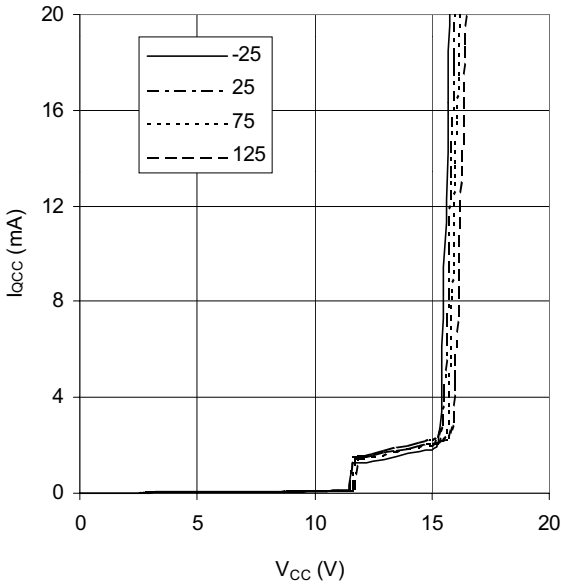
# IR2156(S) & (PbF)



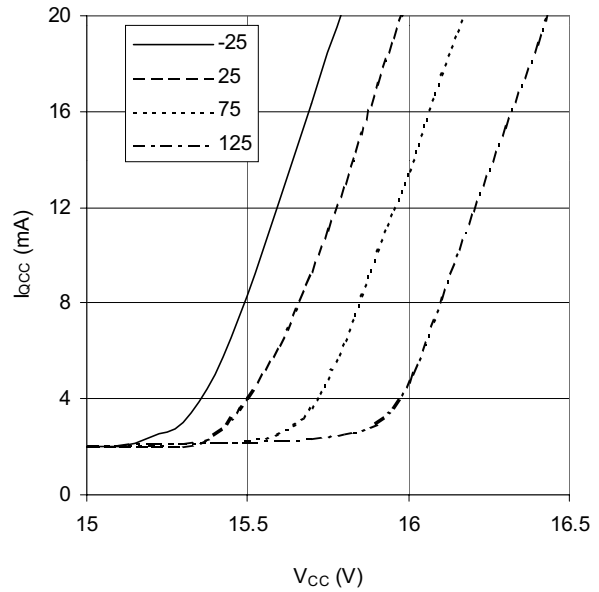
Graph 13. SD+, SD- vs Temperature (IR2156)



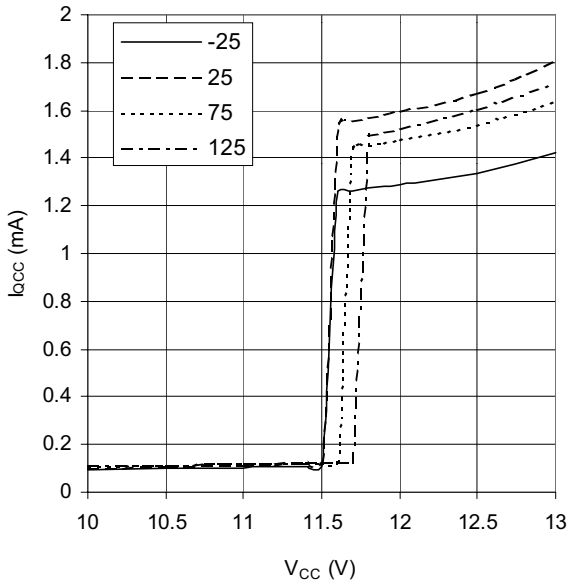
Graph 14. I<sub>LK</sub> vs Temperature (IR2156)



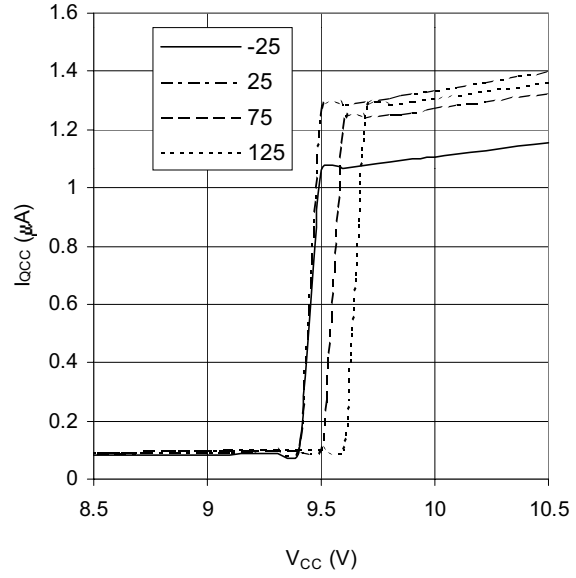
Graph 15. I<sub>QCC</sub> vs V<sub>CC</sub> vs Temperature (IR2156)



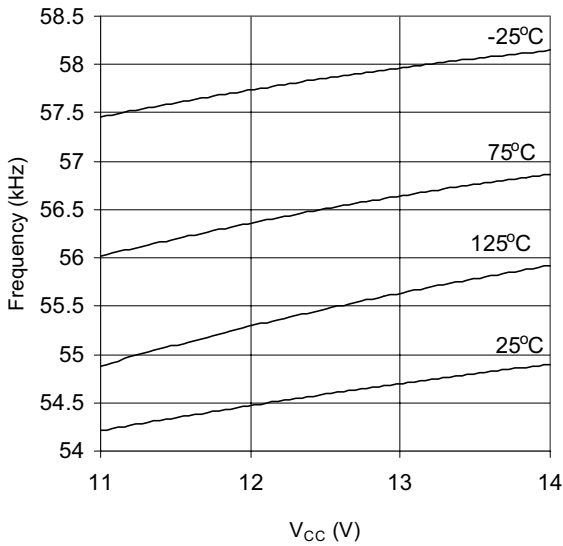
Graph 16. I<sub>QCC</sub> vs V<sub>CC</sub> vs Temperature (IR2156)  
Internal Zener Diode Curve



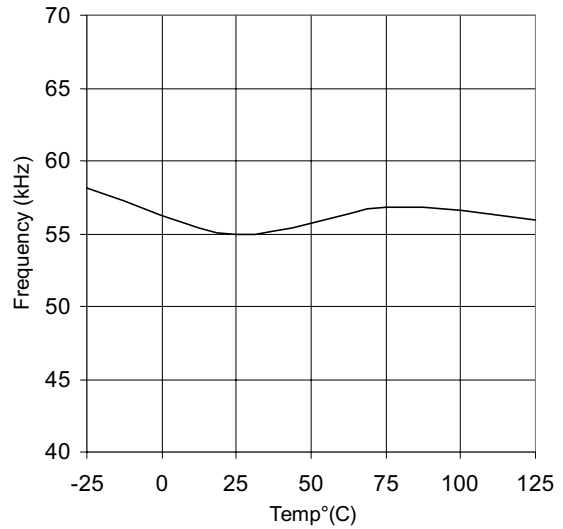
Graph 17.  $I_{QCC}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $V_{CCUV+}$



Graph 18.  $I_{QCC}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $V_{CCUV-}$

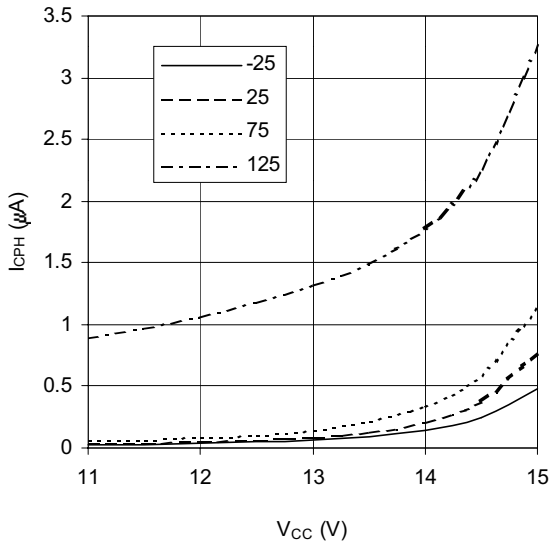


Graph 19.  $F_{OSC}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $V_{CPH} = 0V$

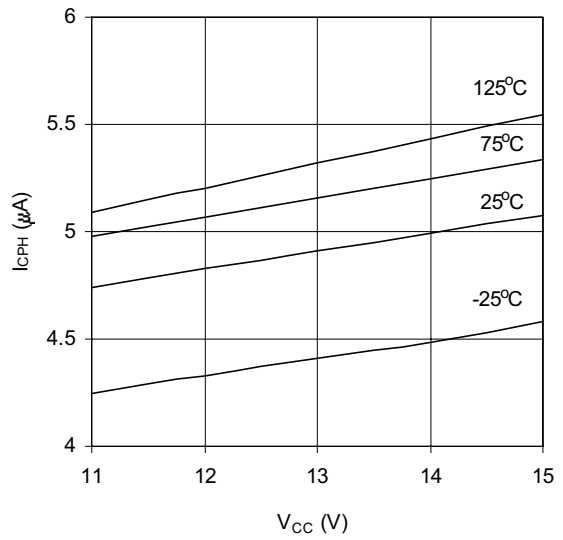


Graph 20.  $F_{OSC}$  vs Temperature (IR2156)  
 $V_{CPH} = 0V$

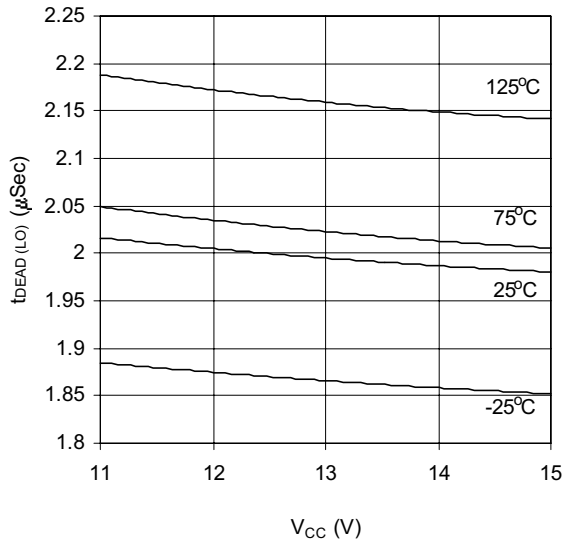
# IR2156(S) & (PbF)



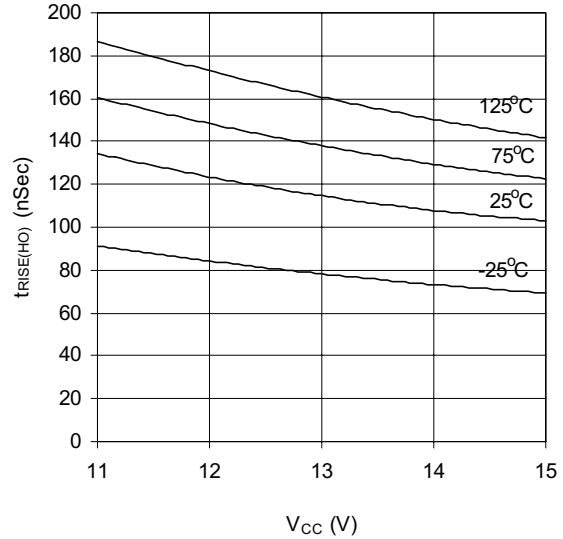
Graph 21.  $I_{CPH}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $V_{CPH} = V_{CC}$



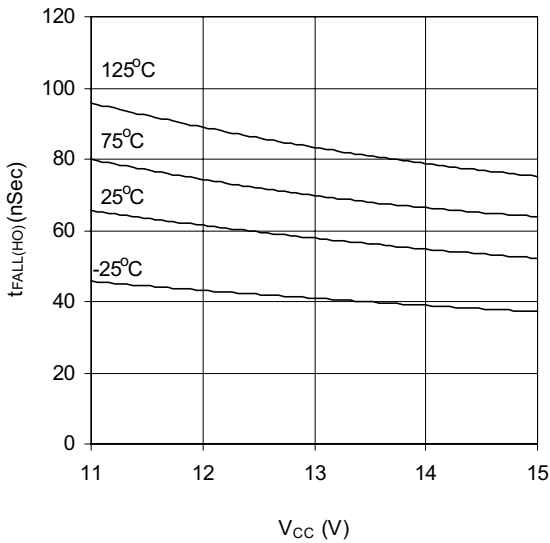
Graph 22.  $I_{CPH}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $V_{CPH} = 0V$



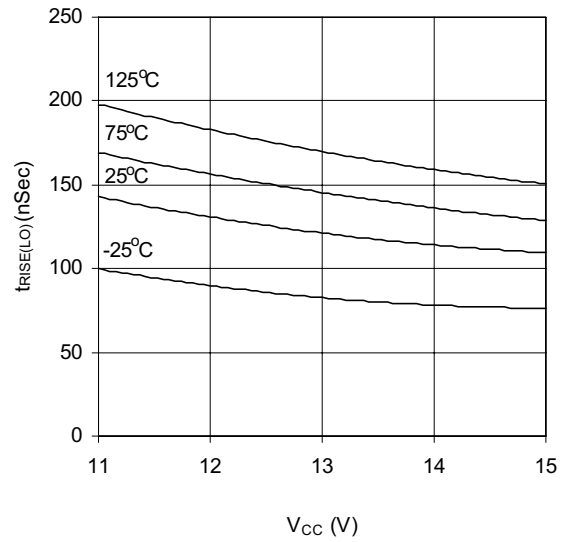
Graph 23.  $t_{DEAD(LO)}$  vs  $V_{CC}$  vs Temperature (IR2156)  
 $C_T = 1nF$



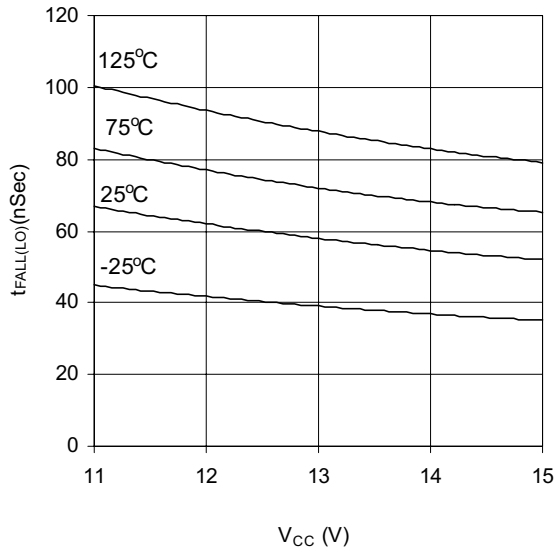
Graph 24.  $t_{RISE(HO)}$  vs  $V_{CC}$  vs Temperature (IR2156)



Graph 25.  $t_{FALL(HO)}$  vs  $V_{CC}$  vs Temperature (IR2156)



Graph 26.  $t_{RISE(LO)}$  vs  $V_{CC}$  vs Temperature (IR2156)



Graph 27.  $t_{FALL(LO)}$  vs  $V_{CC}$  vs Temperature (IR2156)

# IR2156(S) & (PbF)

## Functional Description

### Under-voltage Lock-Out Mode (UVLO)

The under-voltage lock-out mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. To identify the different modes of the IC, refer to the State Diagram shown on page 6 of this document. The IR2156 undervoltage lock-out is designed to maintain an ultra low supply current of less than 200uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. Figure 1 shows an efficient supply voltage using the start-up current of the IR2156 together with a charge pump from the ballast output stage (RSUPPLY, CVCC, DCP1 and DCP2).

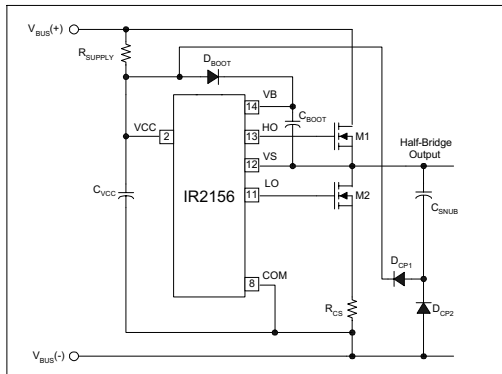


Figure 1, Start-up and supply circuitry.

The start-up capacitor (CVCC) is charged by current through supply resistor (RSUPPLY) minus the start-up current drawn by the IC. This resistor is chosen to provide 2X the maximum start-up current to guarantee ballast start-up at low line input voltage. Once the capacitor voltage on VCC reaches the start-up threshold, and the SD pin is below 4.5 volts, the IC turns on and HO and LO begin to oscillate. The capacitor begins to discharge due to the increase in IC operating current (Figure 2).

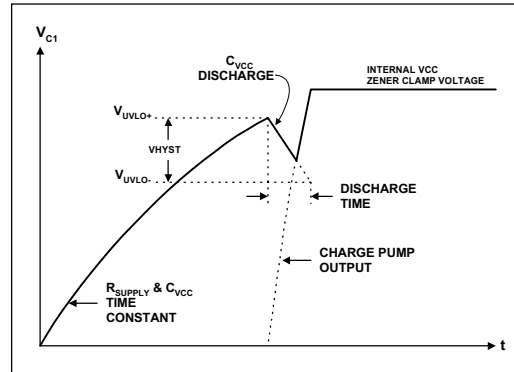


Figure 2, Supply capacitor (CVCC) voltage.

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the IC turn-off threshold. The charge pump and the internal 15.6V zener clamp of the IC take over as the supply voltage. The start-up capacitor and snubber capacitor must be selected such that enough supply current is available over all ballast operating conditions. A bootstrap diode (DBOOT) and supply capacitor (CBOOT) comprise the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During undervoltage lock-out mode, the high- and low-side driver outputs HO and LO are both low, pin CT is connected internally to COM to disable the oscillator, and pin CPH is connected internally to COM for resetting the preheat time.

### Preheat Mode (PH)

The preheat mode is defined as the state the IC is in when the lamp filaments are being heated to their correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. The IR2156 enters preheat mode when VCC exceeds the UVLO positive-going threshold. HO and LO begin to



oscillate at the preheat frequency with 50% duty cycle and with a dead-time which is set by the value of the external timing capacitor, CT, and internal deadtime resistor, RDT. Pin CPH is disconnected from COM and an internal 4 $\mu$ A current source (Figure 3)

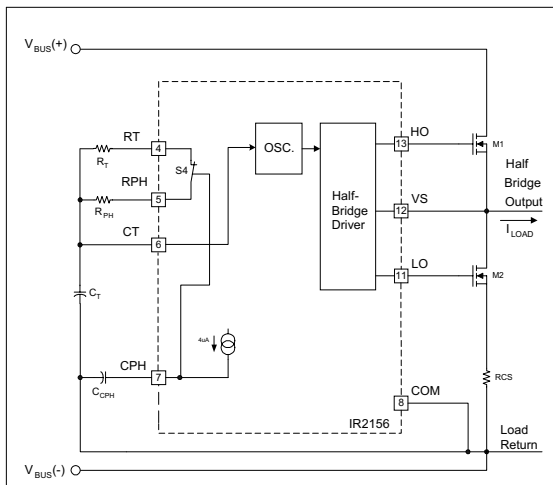


Figure 3, Preheat circuitry.

charges the external preheat timing capacitor on CPH linearly. The over-current protection on pin CS is disabled during preheat. The preheat frequency is determined by the parallel combination of resistors RT and RPH, together with timing capacitor CT. CT charges and discharges between 1/3 and 3/5 of VCC (see Timing Diagram, page 7). CT is charged exponentially through the parallel combination of RT and RPH connected internally to VCC through MOSFET S1. The charge time of CT from 1/3 to 3/5 VCC is the on-time of the respective output gate driver, HO or LO. Once CT exceeds 3/5 VCC, MOSFET S1 is turned off, disconnecting RT and RPH from VCC. CT is then discharged exponentially through an internal resistor, RDT, through MOSFET S3 to COM. The discharge time of CT from 3/5 to 1/3 VCC is the dead-time (both

off) of the output gate drivers, HO and LO. The selected value of CT together with RDT therefore program the desired dead-time (see Design Equations, page 19, Equations 1 and 2). Once CT discharges below 1/3 VCC, MOSFET S3 is turned off, disconnecting RDT from COM, and MOSFET S1 is turned on, connecting RT and RPH again to VCC. The frequency remains at the preheat frequency until the voltage on pin CPH exceeds 13V and the IC enters Ignition Mode. During the preheat mode, both the over-current protection and the DC bus under-voltage reset are enabled when pin CPH exceeds 7.5V.

## Ignition Mode (IGN)

The ignition mode is defined as the state the IC is in when a high voltage is being established across the lamp necessary for igniting the lamp. The IR2156 enters ignition mode when the voltage on pin CPH exceeds 13V.

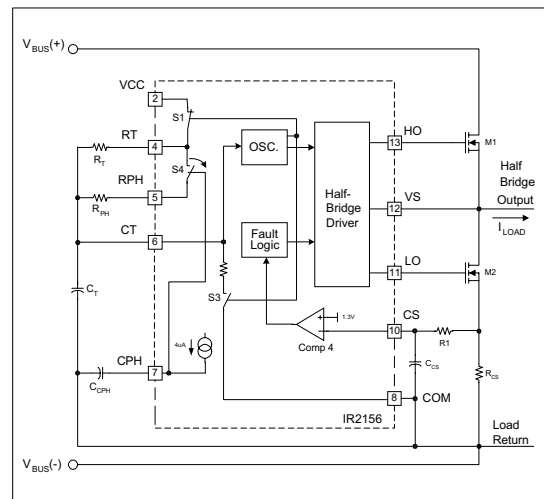


Figure 4, Ignition circuitry.

Pin CPH is connected internally to the gate of a p-channel MOSFET (S4) (see Figure 4) that connects pin RPH with pin RT. As pin CPH

exceeds 13V, the gate-to-source voltage of MOSFET S4 begins to fall below the turn-on threshold of S4. As pin CPH continues to ramp towards VCC, switch S4 turns off slowly. This results in resistor RPH being disconnected smoothly from resistor RT, which causes the operating frequency to ramp smoothly from the preheat frequency, through the ignition frequency, to the final run frequency. The over-current threshold on pin CS will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor RCS. The resistor RCS therefore programs the maximum allowable peak ignition current (and therefore peak ignition voltage) of the ballast output stage. The peak ignition current must not exceed the maximum allowable current ratings of the output stage MOSFETs. Should this voltage exceed the internal threshold of 1.3V, the IC will enter FAULT mode and both gate driver outputs HO and LO will be latched low.

## Run Mode (RUN)

Once the lamp has successfully ignited, the ballast enters run mode. The run mode is defined as the state the IC is in when the lamp arc is established and the lamp is being driven to a given power level. The run mode oscillating frequency is determined by the timing resistor RT and timing capacitor CT (see Design Equations, page 19, Equations 3 and 4). Should hard-switching occur at the half-bridge at any time due to an open-filament or lamp removal, the voltage across the current sensing resistor, RCS, will exceed the internal threshold of 1.3 volts and the IC will enter FAULT mode. Both gate driver outputs, HO and LO, will be latched low.

## DC Bus Under-voltage Reset

Should the DC bus decrease too low during a brown-out line condition or over-load condition, the resonant output stage to the lamp can shift near or below resonance. This can produce hard-switching at the half-bridge which can damage the half-bridge switches. To protect against this, pin VDC measures the DC bus voltage and pulls down on pin CPH linearly as the voltage on pin VDC decreases 10.9V below VCC. This causes the p-channel MOSFET S4 (Figure 4) to close as the DC bus decreases and the frequency to shift higher to a safe operating point above resonance. The DC bus level at which the frequency shifting occurs is set by the external RBUS resistor and internal RVDC resistor. By pulling down on pin CPH, the ignition ramp is also reset. Therefore, should the lamp extinguish due to very low DC bus levels, the lamp will be automatically ignited as the DC bus increases again. The internal RVDC resistor is connected between pin VDC and COM when CPH exceeds 7.5V (during preheat mode).

## Fault Mode (FAULT)

Should the voltage at the current sensing pin, CS, exceed 1.3 volts at any time after the preheat mode, the IC enters fault mode and both gate driver outputs, HO and LO, are latched in the 'low' state. CPH is discharged to COM for resetting the preheat time, and CT is discharged to COM for disabling the oscillator. To exit fault mode, VCC must be recycled back below the UVLO negative-going turn-off threshold, or, the shutdown pin, SD, must be pulled above 5.1 volts. Either of these will force the IC to enter UVLO mode (see State Diagram, page 6). Once VCC is above the turn-on threshold and SD is below 4.5 volts, the IC will begin oscillating again in the preheat mode.

## Design Equations

Note: The results from the following design equations can differ slightly from experimental measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

### Step 1: Program Dead-time

The dead-time between the gate driver outputs HO and LO is programmed with timing capacitor CT and an internal dead-time resistor RDT. The dead-time is the discharge time of capacitor CT from 3/5VCC to 1/3VCC and is given as:

$$t_{DT} = C_T \cdot 2000 \quad [\text{Seconds}] \quad (1)$$

or

$$C_T = \frac{t_{DT}}{2000} \quad [\text{Farads}] \quad (2)$$

### Step 2: Program Run Frequency

The final run frequency is programmed with timing resistor RT and timing capacitor CT. The charge time of capacitor CT from 1/3VCC to 3/5VCC determines the on-time of HO and LO gate driver outputs. The run frequency is therefore given as:

$$f_{RUN} = \frac{1}{2 \cdot C_T (0.6 \cdot R_T + 2000)} \quad [\text{Hertz}] \quad (3)$$

or

$$R_T = \frac{1}{1.12 \cdot C_T \cdot f_{RUN}} - 3333 \quad [\text{Ohms}] \quad (4)$$

### Step 3: Program Preheat Frequency

The preheat frequency is programmed with timing resistors RT and RPH, and timing capacitor CT. The timing resistors are connected in parallel internally for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{PH} = \frac{1}{2 \cdot C_T \cdot \left( \frac{0.6 \cdot R_T \cdot R_{PH}}{R_T + R_{PH}} + 2000 \right)} \quad [\text{Hertz}] \quad (5)$$

or

$$R_{PH} = \frac{\left( \frac{1}{1.12 \cdot C_T \cdot f_{PH}} - 3333 \right) \cdot R_T}{R_T - \left( \frac{1}{1.12 \cdot C_T \cdot f_{PH}} - 3333 \right)} \quad [\text{Ohms}] \quad (6)$$

### Step 4: Program Preheat Time

The preheat time is defined by the time it takes for the capacitor on pin CPH to charge up to 13 volts (assuming Vcc = 15 volts). An internal current source of 4.3µA flows out of pin CPH. The preheat time is therefore given as:

$$t_{PH} = C_{PH} \cdot 3.02e6 \quad [\text{Seconds}] \quad (7)$$

or

$$C_{PH} = t_{PH} \cdot 0.331e-6 \quad [\text{Farads}] \quad (8)$$

### Step 5: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor RCS and an internal threshold of 1.25 volts. This threshold determines the over-current limit of the ballast, which can be exceeded when the frequency ramps down towards resonance during ignition and the lamp does not

# IR2156(S) & (PbF)

ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{1.25}{R_{CS}} \quad [\text{Amps Peak}] \quad (9)$$

or

$$R_{CS} = \frac{1.25}{I_{IGN}} \quad [\text{Ohms}] \quad (10)$$

## Design Example: 42W-QUAD BIAx CFL

Note: The results from the following design example can differ slightly from experimental results due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

### Step 1: Program Dead-time

The dead-time is chosen to be 0.8μs. Using Equation (2) gives the following result:

$$C_T = \frac{t_{DT}}{2000} = \frac{0.8e-6}{2000} = 400pF \Rightarrow 470pF$$

### Step 2: Program Run Frequency

The run frequency is chosen to be 43kHz. Using Equation (4) gives the following result:

$$R_T = \frac{1}{1.12 \cdot C_T \cdot f_{RUN}} - 3333$$

$$R_T = \frac{1}{1.12 \cdot 470 pF \cdot 43000} - 3333$$

$$R_T = 40,846 \Omega \Rightarrow 43k\Omega$$

### Step 3: Program Preheat Frequency

The preheat frequency is chosen such that the lamp filaments are adequately heated within the preheat time. A preheat frequency of 70kHz was chosen. Using Equation (6) gives the following result:

$$R_{PH} = \frac{\left( \frac{1}{1.12 \cdot C_T \cdot f_{PH}} - 3333 \right) \cdot R_T}{R_T - \left( \frac{1}{1.12 \cdot C_T \cdot f_{PH}} - 3333 \right)}$$

$$R_{PH} = \frac{\left( \frac{1}{1.12 \cdot 470 pF \cdot 70000} - 3333 \right) \cdot 43000}{43000 - \left( \frac{1}{1.02 \cdot 470 pF \cdot 70000} - 3333 \right)}$$

$$R_{PH} = 53,330\Omega \Rightarrow 51k\Omega$$

### Step 4: Program Preheat Time

The preheat time of 500ms seconds was chosen. Using Equation (8) gives the following result:

$$C_{PH} = t_{PH} \cdot 0.331e-6$$

$$C_{PH} = (500e-3) \cdot (0.331e-6)$$

$$C_{PH} = 0.166\mu F - > 0.22\mu F$$

### Step 5: Program Ignition Current

The maximum ignition current is given by the maximum ignition voltage and is chosen as 2.0Apk. Using Equation (10) gives the following result:

$$R_{CS} = \frac{1.25}{I_{IGN}}$$

$$R_{CS} = \frac{1.3}{2.0} = 0.625\text{Ohms} \Rightarrow 0.61\text{Ohms}$$

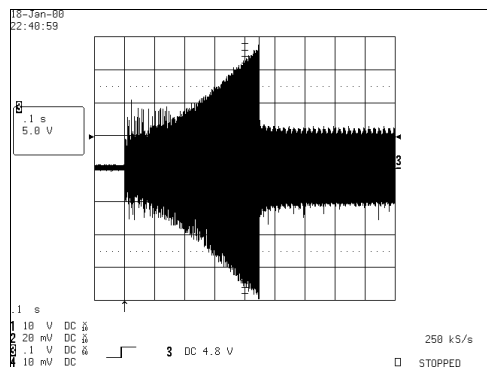
### Results

A fully-functional ballast was designed, built and tested using the calculated values. The values were then adjusted slightly in order to fulfill various ballast parameters (Table 1). The ballast was designed using the 'Typical Application Schematic' given on page 1.

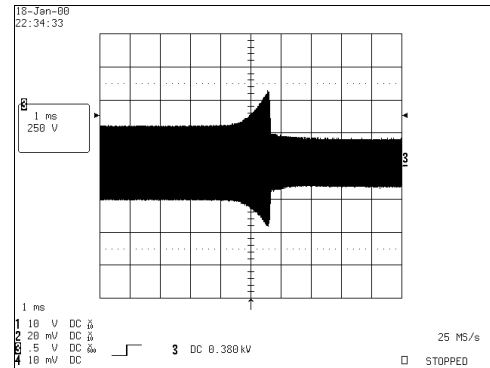
Parameter	Description	Value
fph	Preheat Frequency	68kHz
Vph	Lamp Preheat Voltage	460Vpp
tph	Preheat Time	700ms
Rw:Rc	Filament Preheat Ratio	4:1
Vign	Maximum Ignition Voltage	1500Vpp
tign	Ignition Ramp Time	50ms
frun	Running Frequency	47.5kHz
Vrun	Running Lamp Voltage	180Vpk
Pin	Running Ballast Input Power	42W

Table 1, 42W-Quad Biax Ballast Measured Results

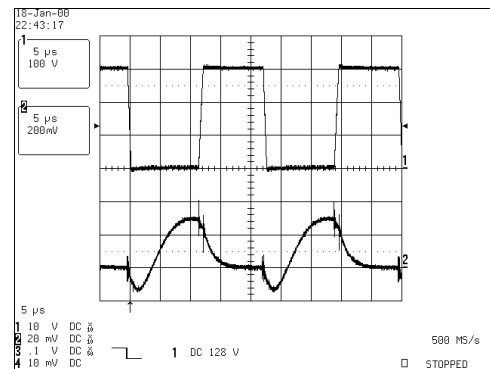
### Waveforms



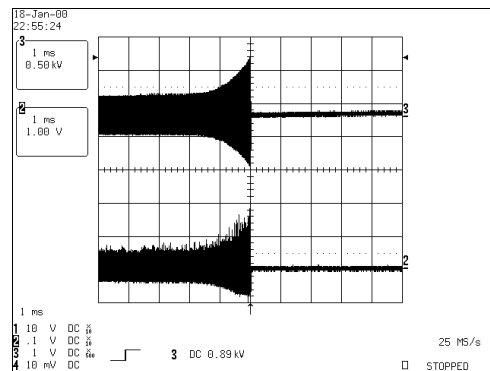
Waveform 1. Lamp filament voltage during preheat



Waveform 2. Lamp voltage during preheat, ignition and run modes



Waveform 3, Half-bridge and current sense voltage during run mode

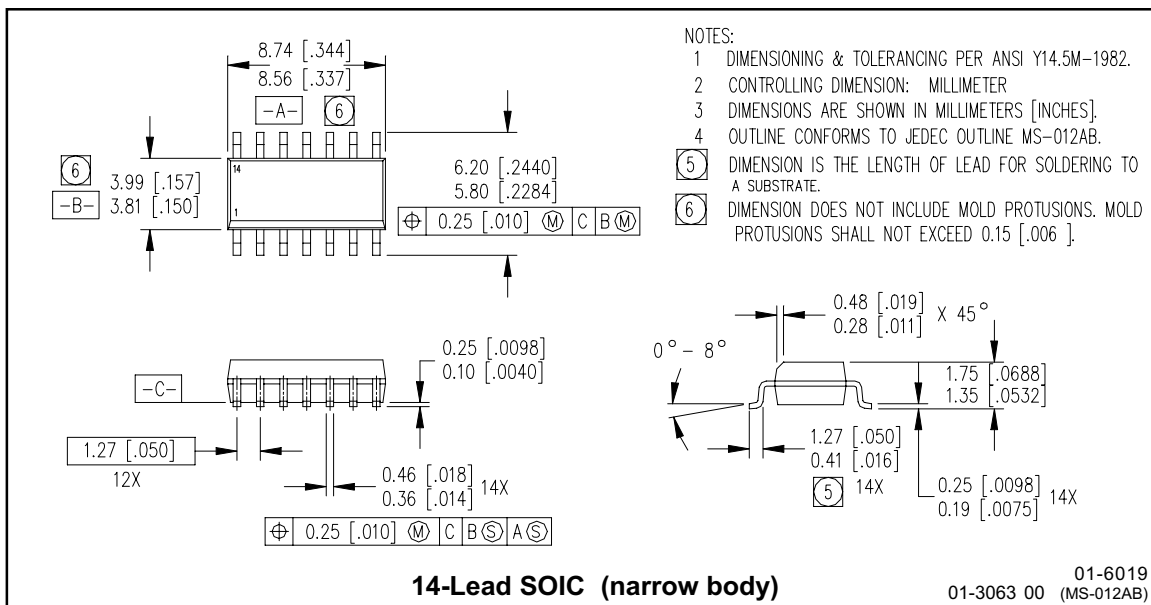
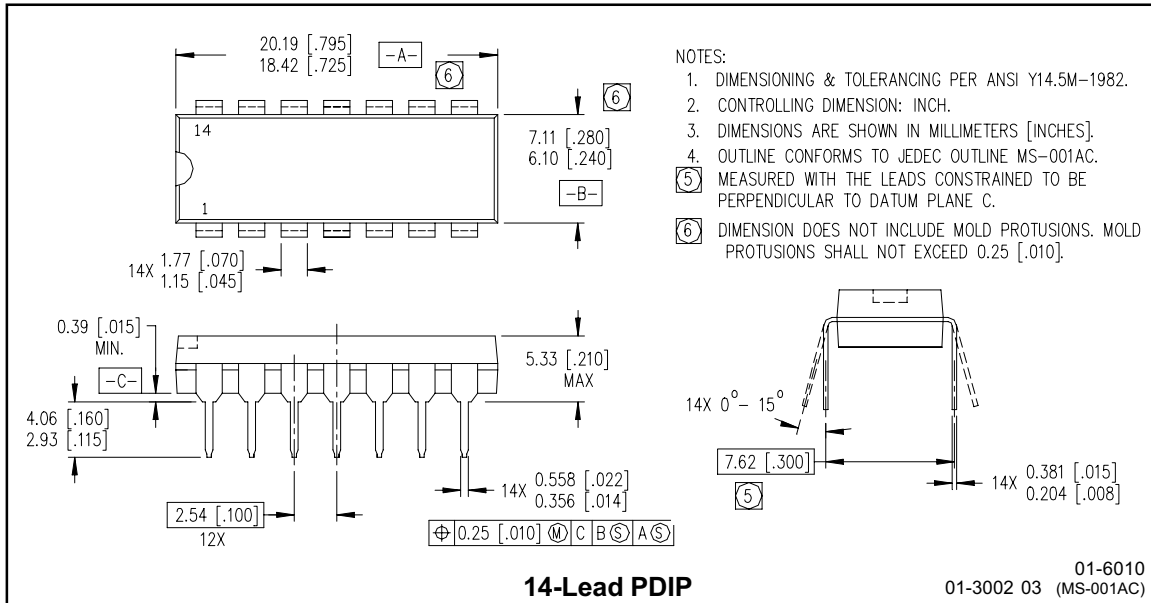


Waveform 4, Lamp voltage and current sense pin during a failure-to-strike lamp fault condition.

# IR2156(S) & (PbF)

International  
**IRF** Rectifier

## Case outline



## Bill Of Materials

Schematic: Typical Application Diagram, Page 1

Lamp Type: 42W-Quad Biax

Line Input Voltage: 120VAC

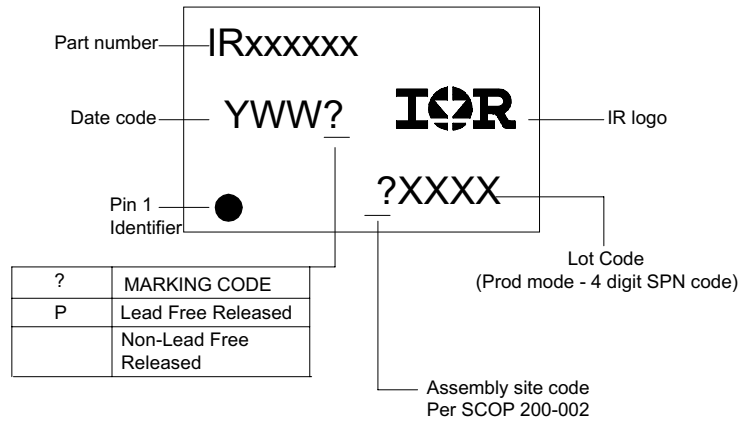
Item	Qty	Description	Designator	Value	Manufacturer	Part No.
1	1	Fuse	F1			
2	1	Filter Capacitor	CFILTER	0.1 $\mu$ F/400V		
3	1	Filter Inductor	LFILTER	330 $\mu$ H/0.5A		
4	2	Rectifier Diode	DRECT1, DRECT2	1N4007		
5	2	Electrolytic Capacitor	CELCAP1, CELCAP2	47 $\mu$ F/250V		
6	1	Resonant Inductor	LRES	1.25mH/1.5A		
7	1	Charge Pump Capacitor	CCP	470pF/1kV		
8	2	Charge Pump Diodes	DCP1, DCP2	1N4148		
9	1	Resonant Capacitor	CRES	6.8nF/1kV		
10	1	Snubber Capacitor	CSNUB	470pF/1kV		
11	2	Half-Bridge MOSFET	M1, M2	IRF730		
12	1	Current Sense Resistor	RCS	0.75R/0.5W		
13	1	Limit Resistor	R1	1k/0.25W		
14	1	Filter Capacitor	CCS	470pF/16V		
15	2	Supply Capacitor	CBOOT, CVCC1	0.1 $\mu$ F/25V		
16	1	Supply Capacitor	CVCC2	2.2 $\mu$ F/25V		
17	1	Bootstrap Diode	DBOOT	10DF6		
18	1	Ballast Control IC	IC1	IR2156		
19	2	Resistor	RSUPPLY, RBUS	1M/0.25W		
20	1	Timing Resistor	RT	39k/0.25W		
21	1	Timing Capacitor	CT	470pF/25V		
22	1	Preheat Resistor	RPH	75k/0.25W		
23	1	Preheat Capacitor	CPH	0.22 $\mu$ F/25V		
24	1	Capacitor	CVDC	0.01 $\mu$ F/25V		
TOTAL	30					

Device qualified to Industrial Level

# IR2156(S) & (PbF)

International  
**IR** Rectifier

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

### Basic Part (Non-Lead Free)

14-Lead PDIP IR2156 order IR2156  
14-Lead SOIC IR2156S order IR2156S

### Leadfree Part

14-Lead PDIP IR2156 order IR2156PbF  
14-Lead SOIC IR2156S order IR2156SPbF

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**IR** Rectifier

This product has been designed and qualified for the industrial market.

Qualification Standards can be found on IR's Web Site <http://www.irf.com>

Data and specifications subject to change without notice.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

10/25/2004